WHAT IS CLAIMED IS:

1. A motor drive system comprising:

an input for alternating current;

a rectifier circuit operative to convert the input alternating current to direct current;

an inverter circuit operable to convert the direct current to PWM current pulses at a selected frequency and a controllable duty cycle for driving a motor;

a PWM control circuit responsive to signals representative of the motor drive current and to a carrier signal at the selected frequency to operate the inverter; and

a motor drive current sensing circuit which provides a control input to the PWM control circuit, and which includes an input filter operative to block noise components of the motor drive current signal, wherein:

the input filter is comprised of an integration circuit, and is driven by a triggering signal at a frequency which is an integer multiple of the selected frequency.

2. A motor drive system as described in claim 1, wherein the triggering signal is derived from a SYNC signal at the selected frequency, and which has a predetermined phase relationship to the carrier signal.

3. A motor drive system as described in claim 2, wherein the carrier signal is a triangular wave, the SYNC signal is a square wave, and the triggering signal is derived from level transitions of the square wave at zero crossings of the triangular wave, or at direction transitions of the triangular wave.

4. A motor drive system as described in claim 1, wherein the integration circuit triggering signal frequency is twice the selected frequency.

5. A motor drive system as described in claim 4, wherein the integration circuit is comprised of:

a first integrator coupled directly to the motor drive current signal;

a second integrator coupled to the motor drive current signal through a delay circuit which introduces a delay equal to the period of the integration circuit triggering signal; and the filter further includes:

a subtraction circuit coupled to outputs of the first and second integrators; and

a sample and hold circuit operated at the integration circuit triggering signal frequency.

6. A motor drive system as described in claim 5, wherein the integration circuit is operative to suppress even harmonics of the selected frequency.

7. A motor drive system as described in claim 5, wherein the sample and hold circuit is operative to suppress the selected frequency and odd harmonics thereof.

8. A motor drive system as described in claim 7, further including a circuit operative to determine the mean value of two successive outputs of the sample and hold circuit.

9. A motor drive system as described in claim 4, wherein:

the integration circuit is comprised of a voltage-to-time converter including:

an integrator;

a first switching element which couples the motor drive current signal to an input of the integrator; and

a second switching element which couples a reference signal to the integrator input;

the reference signal is opposite in polarity to the motor drive current signal;

the first switching element is alternatingly turned on and off for successive first and second intervals equal to the period of the integration circuit triggering signal;

the second switching element is turned off during the first interval and is turned on during the second interval;

the input filter further includes a level detector operative to provide an indication when an output from the integration circuit returns to a predetermined level during the second interval equal to the level at the beginning of the first interval.

10. A motor drive system as described in claim 9, wherein the integration circuit is further comprised of a second voltage to time converter including:

a second integrator;

a third switching element which couples the motor drive current signal to an input of the second integrator; and

a fourth switching element which couples the reference signal to the input of the second integrator; wherein:

the third switching element is alternatingly turned on during the second interval and turned off during the first interval;

the fourth switching element is turned on during the first interval and is turned off during the second interval; and

the level detector is operative to provide an indication when an output from the second integrator returns to a second predetermined level during the first interval equal to the level at the beginning of the second interval.

11. A motor drive system as described in claim 10, wherein the level detector is a zero-crossing detector.

12. A motor drive system as described in claim 4, wherein the integration circuit includes a switched capacitor integrator operated by switching pulses synchronized with the triggering signal, the switching pulses having a frequency which is a high multiple of the selected frequency.

13. A motor drive system as described in claim 12, further including a sampling switch connected between an output of the integrator and an input of an analog to digital converter, the sampling switch being operated at the frequency of the integration circuit triggering signal.

14. A motor drive system as described in claim 13, further including a delay circuit connected to an output of the analog to digital converter, and a summing circuit operative to add the delayed and undelayed outputs of the analog to digital converter

15. A motor drive system as described in claim 14, wherein the current sensing circuit further includes:

a resistance element in series between an output of the inverter and the motor; and

a circuit for measuring the voltage drop across the resistance element.

16. A motor drive system as described in claim 1, wherein:

the motor drive system is operative to drive a multi-phase motor;

the inverter circuit is operable to provide current pulses in a predetermined phase relationship for each phase of the motor at the selected frequency and the controllable duty cycle;

the control circuit is responsive to signals representative of the motor drive current for each phase of the motor; and

the motor drive current sensing circuit includes an input filter for each of the motor drive phase current signals.

17. An input filter for eliminating ripple noise in a phase current sensing circuit for a PWM motor drive system which provides motor drive signals in the form of current pulses derived from a carrier signal at a selected frequency and a controllable duty cycle for driving a motor,

the filter being comprised of an integration circuit driven by a triggering signal at a frequency which is an integer multiple of the selected frequency.

18. An input filter as described in claim 17, wherein the triggering signal is derived from a SYNC signal at the selected frequency, and which has a predetermined phase relationship to the carrier signal.

19. An input filter as described in claim 18, wherein the carrier signal is a triangular wave, the SYNC signal is a square wave, and the triggering signal is derived from level transitions of the square wave at zero crossings of the triangular wave, or at direction transitions of the triangular wave.

20. An input filter as described in claim 17, wherein the integration circuit triggering signal frequency is twice the selected frequency.

21. An input filter as described in claim 20, wherein the integration circuit is comprised of:

a first integrator coupled directly to the motor drive current signal;

a second integrator coupled to the motor drive current signal through a delay circuit which introduces a delay equal to the period of the integration circuit triggering signal; and the filter further includes:

a subtraction circuit coupled to outputs of the first and second integrators; and

a sample and hold circuit operated at the integration circuit triggering signal frequency.

22. An input filter as described in claim 21, wherein the integration circuit is operative to suppress even harmonics of the selected frequency.

23. An input filter as described in claim 21, wherein the sample and hold circuit is operative to suppress the selected frequency and odd harmonics thereof.

24. An input filter as described in claim 23, further including a circuit operative to determine the mean value of two successive outputs of the sample and hold circuit.

25. An input filter as described in claim 20, wherein:

the integration circuit is comprised of a voltage-to-time converter including:

an integrator;

a first switching element which couples the motor drive current signal to an input of the integrator; and

a second switching element which couples a reference signal to the integrator input;

the reference signal is opposite in polarity to the motor drive current signal;

the first switching element is alternatingly turned on and off for successive first and second intervals equal to the period of the integration circuit triggering signal;

the second switching element is turned off during the first interval and is turned on during the second interval;

the input filter further includes a level detector operative to provide an indication when an output from the integration circuit returns to a predetermined level during the second interval equal to the level at the beginning of the first interval.

26. An input filter as described in claim 25, wherein the integration circuit is further comprised of a second voltage to time converter including:

a second integrator;

a third switching element which couples the motor drive current signal to an input of the second integrator; and

a fourth switching element which couples the reference signal to the input of the second integrator; wherein:

the third switching element is alternatingly turned on during the second interval and turned off during the first interval;

the fourth switching element is turned on during the first interval and is turned off during the second interval; and

level detector is operative to provide an indication when an output from the second integrator returns to a second predetermined level during the first interval equal to the level at the beginning of the second interval.

27. An input filter as described in claim 26, wherein the level detector is a zero-crossing detector.

28. An input filter as described in claim 20, wherein the integration circuit includes a switched capacitor integrator operated by switching pulses synchronized with the triggering signal, the switching pulses having a frequency which is a high multiple of the selected frequency.

29. An input filter as described in claim 28, further including a sampling switch connected between an output of the integrator and an input of an analog to digital converter, the sampling switch being operated at the frequency of the integration circuit triggering signal.

30. An input filter as described in claim 29, further including a delay circuit connected to an output of the analog to digital converter, and a summing circuit operative to add the delayed and undelayed outputs of the analog to digital converter.